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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/631,173 | 07/31/2003 | Diego F. Vila | CROSS1520 | 1418 |

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| EXAMINER | |
|---|---|
| TRAN, KHAI | |

| ART UNIT | PAPER NUMBER |
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| 2611 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/631,173 | VILA ET AL. | |
| | Examiner | Art Unit | |
| | KHAI TRAN | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-6* is/are allowed.

6)☒ Claim(s) *7-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/17/2007 has been entered. Claims 6, 18 have been cancelled. Claims 1-5, 7-17, and 19-23 are pending in this Office action.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 7-17, 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Webb et al (U.S. Pat. 4,855,735) in view of Wilkinson (U.S. Pat. 4,543,657).

Regarding claim 7, Webb et al. discloses a system comprising: a receiver shift register (40 in Fig. 1 and col. 4, lines 18-19); and a feedback circuit coupled to the receiver shift register (col. 6, lines 42-48, wherein, 'output means being connected to the input means for recirculating data bits' is interpreted as equivalent to the feedback circuit); wherein one or more cells of the receiver shift register are configured to alternatively accept as input either a bit from a preceding cell or a received bit of

synchronization data from a transmitter (col. 5, lines 25-29 and lines 7-21) wherein the synchronization data corresponds to at least one bit from a corresponding transmitter shift register (col. 5, lines 25-29, and col. 6, lines 64-68). Webb et al fail to disclose wherein the receiver shift register generates a pseudorandom bit sequence used to identify the occurrence of errors in a data transmission from the transmitter.

Wilkinson discloses wherein the receiver shift register generates a pseudo-random bit sequences used to identify the occurrence of errors in a data transmission from the transmitter (col. 2, lines 41-47, col. 3, lines 19-32, col. 3, lines 22-27). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the method of identifying the occurrence of errors as taught by Wilkinson into the teachings of Webb et al, in order to determine the bit error rate of the channel, and therefore, reliability of received data.

Regarding claim 8, Wilkinson discloses, further comprising a counter coupled to the receiver shift register, wherein the counter is configured to assert a "synchronized" signal when a predetermined count is reached after a reset event (Column 6 Lines 36-41).

Regarding claim 9, Wilkinson further discloses, wherein the predetermined count corresponds to the receiver shift register being filled with synchronization data (Column 6 Lines 36-43, wherein, "Fill" is equivalent to filled with synchronization data).

Regarding claim 10, Webb et al. discloses, wherein the one or more cells of the receiver shift register are configured to accept received bits of synchronization data as input until the receiver shift register is filled with synchronization data, and to accept bits

from preceding cells as input when the receiver shift register is filled with synchronization data (Column 5 Lines 3-21, Column 4 Lines 29-31, and Column 3 Lines 11-12, wherein, it is understood that recirculation is propagation of a bit from one flip-flop of the shift register to another).

Regarding claim 11, Webb et al. discloses, wherein upon occurrence of a reset event, data in the receiver shift register is invalid data (Column 4 Lines 58-60)..

Regarding claim 12, Wilkinson further discloses, further comprising one or more demultiplexers coupled to provide input to the one or more cells, wherein the one or more demultiplexers are configured to select either bits from preceding cells or received bits of synchronization data to provide as input to the one or more cells (col. 2, line 64 to col. 3, line 2, wherein, switching means is interpreted as demultiplexers, and shift register comprises preceding cells, as discussed above).

Regarding claim 13, Wilkinson further discloses, wherein the demultiplexers are coupled to receive an indication of whether the receiver shift register is synchronized (col. 2, lines 61-63).

Regarding claim 14, Wilkinson further discloses, wherein the demultiplexers are coupled to a counter, wherein the counter is configured to provide the indication when a predetermined count is reached after a reset event (col. 6, lines 36-41 ).

Regarding claim 15, Webb et al. discloses, further comprising a transmission medium coupled to the receiver shift register (col. 3, lines 50-52 and in Fig. 1 'PARALLEL DATA WORD' coupled to the shift register 40).

Regarding claim 16, Webb et al. discloses, wherein the transmission medium is configured to transport the synchronization data in idle codes (Column 7 Lines 17-20, wherein, the data clock signal is interpreted as the idle codes. Also, see claim 15 above).

Regarding claim 17, Wilkinson further discloses, wherein the transmitter shift register configured to generate a first bit sequence, and the receiver shift register is configured to generate an identical bit sequence (col. 6, lines 1-6 and col. 11, lines 38-41).

Regarding claim 19, Webb et al. discloses the system of claim 7, wherein the receiver shift register is configured to load synchronization data on each cycle into one or more predetermined cells of the receiver shift register (col.8, lines 1-8).

Regarding claim 20, Webb et al. discloses the system of claim 19, wherein the one or more predetermined cells of the receiver shift register exclude at least one of the cells of the receiver shift register (col. 3, lines 54-58 and col. 6, lines 42-48, wherein, when number of bits n is chosen to be greater than the number of bits in the converted 8 bit binary number, i.e., when n is chosen to be 9 or greater, predetermined cells will exclude at least one of the cells of the receiver Shift register).

Regarding claim 21, Webb et al. discloses the system of claim 20, wherein the receiver shift register cells comprise 11 serially coupled flip-flops and wherein the predetermined cells comprise 8 consecutive ones of the 11serially coupled flip-flops (col. 3, lines 54-58 and col. 6, lines 42-48, wherein, n is chosen to be 11).

Regarding claim 23 is similar to claim 7. Therefore, claim 23 is rejected under a similar rationale.

***Claim Rejections - 35 USC § 103***

4. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Webb et al (U.S. Pat. 4,855,735) in view of Wilkinson (U.S. Pat. 4,543,657) and further in view of Nozuyama (U.S. Pat. 5,867,409).

Regarding claim 22, Webb et at and Wilkinson do not disclose, wherein the feedback circuit comprises an exclusive OR (XOR) gate having two inputs coupled to receive the outputs of two of the cells of the receiver shift register, the XOR gate further having an output that is coupled to the input of a first cell of the receiver shift register. However, Nozuyama discloses, wherein the feedback circuit comprises an exclusive OR (XOR) gate having two inputs coupled to receive the outputs of two of the cells of the receiver shift register, the XOR gate further having an output that is coupled to the input of a first cell of the receiver shift register (30 in Fig. 3, wherein, XOR gate output is coupled to flip-flop 1).

It is essential that an XOR gate be used in Webb et al.'s feedback register. Use of the XOR gate allows the formation of two or more flip-flops in the feedback circuit (See Nozuyama, Column 5 Lines 43-46). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include an XOR gate, as Nozuyama teaches, in the feedback circuit of Webb et al. and Wilkinson in order to allow the formation of two or more flip-flops.

***Allowable Subject Matter***

5. Claims 1-6 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: none of the prior art discloses the method, comprising: if the receiver shift register is filled with synchronization data, initiating synchronized operation of the receiver shift register with a the corresponding transmitter shift register, wherein during synchronized operation, a bit sequence generated by the receiver shift register is compared to a received bit sequence to identify the occurrence of errors in a data transmission from the transmitter; and if the receiver shift register is not filled with synchronization data, shifting the loaded synchronization data and loading one or more additional bits of synchronization data into the receiver shift register.

***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAI TRAN whose telephone number is (571) 272-3019. The examiner can normally be reached on 7:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KHAI TRAN
Primary Examiner
Art Unit 2611

*KT*
*December 19, 2007*